

ISSCC SPECIAL EVENING TOPIC SESSIONS

- ISSCC'03
- ISSCC'02

SPECIAL TOPIC SESSIONS - 2003

SE1: Highlights of DAC

Organizer/Chair: Steve Molloy, Chief Architect, Netergy Microelectronics, Santa Clara, CA

Co-Chair: Joseph Williams, Distinguished Member of Technical Staff, Agere Systems, Holmdel, NJ

Topics: Challenges in Achieving First-Silicon Success for 10MGate SoCs: A Silicon Engineering Perspective

Aurangzeb Khan, Cadence Design Systems, Sunnyvale, CA

A Universal Technique for Fast and Flexible Instruction-Set Architecture Simulation

Achim Nohl, Aachen University of Technology, Aachen, Germany

Fast and Accurate Behavioral Simulation of Fractional-N Frequency Synthesizers and Other PLL/DLL Circuits

Michael H. Perrott, Asst. Prof., Massachusetts Institute of Technology, Cambridge, MA

An Efficient Optimization-Based Technique to Generate Posynomial Performance Models for Analog Integrated Circuits

Walter P. Daems, Katholieke Univ., Leuven, Belgium

Georges Gielen, Katholieke Univ., Leuven, Belgium

Willy Sansen, Katholieke Univ., Leuven, Belgium

SE2: Circuits in Emerging Technologies

Organizer: Werner Simbuerger, Infineon, Corporate Research, Munich, Germany

Chair: Ian Young, Intel, Logic Technology Development, Hillsboro, OR

Topics: CMOS High-Speed Broadband Techniques

Michael Green, Prof., University of California, Irvine, CA

Design of SiGe Bipolar Circuits for 40 Gb/s Applications

Herbert Knapp, Infineon Technologies, Munich, Germany

Indium-Phosphide Bipolar Integrated Circuits: 40GHz and Beyond
Mark Rodwell, University of California, Santa Barbara, CA

The Double-Gate FinFET: Device Impact on Circuit Design
Ingo Aller, IBM Entwicklung GmbH, Boeblingen, Germany

Carbon Nanotubes: From Synthesis to Integration
Hongile Dai, Associate Professor, Stanford University, CA

SE3: How Far Can Integration Go for 3G Cellphones?
Organizer: William O. Camp, Jr., Senior Scientist, Sony Ericsson Mobile Communications, Research Triangle Park, NC
Chair: Trudy Stetzler, Senior Member of the Technical Staff, Texas Instruments, Stafford, TX

Topics: System Requirements and Integration Trends
Sven Mattisson, Analog Systems Design, Ericsson, Lund, Sweden

Integration of Analog, Digital and Power Regulation on a Chip
James Milke, Motorola, Tempe, AZ

Advanced RF Integration
William Krenik, Texas Instruments, Dallas, TX

Challenges and Future Trends
John Long, Delft University of Technology, Delft, The Netherlands

SPECIAL TOPIC SESSIONS - 2002

SE1: Inductance: Implications and Solutions for High-Speed Digital Circuits

Co-organizer/Co-chair: William J. Bowhill, Intel Corp., Shrewsbury, MA
Co-organizer: Anantha Chandrakasan, MIT, Cambridge, MA
Co-chair: Stephen Kosonocky, IBM, Yorktown Heights, NY

Topics: Inductance Extraction and Modeling
David Blaauw, Univ. of Michigan
Kaushik Gala, Motorola Inc., Austin, TX

On-Chip Signaling
Shannon Morton, Silicon Graphics, Boston, MA

Clock Distribution
Phillip Restle, IBM, Yorktown Heights, NY

Xuejue Huang, Univ. of California-Berkeley, CA

The Chip Interface

Claude Gauthier, Sun Microsystems, Sunnyvale, CA

Brian Amick, Sun Microsystems, Austin, TX

SE2: Low-Voltage Design for Portable Systems

Organizer/Co-chair: Wanda Gass, Texas Instruments, Dallas, TX

Co-chair: Thucydides Xanthopoulos, Cavium Networks, Marlboro, MA

Topics: Technology, Architecture and Applications

Robert Brodersen, Prof., Univ. of California-Berkeley, CA

When MOSFET Switches Become MISFET Dimmers

Dennis Buss, Vice President, Texas Instruments, Dallas, TX

RF Circuits at Low Voltage

Asad Abidi, Prof., Univ. of California-Los Angeles, CA

Leakage Reduction in Digital CMOS Circuits

Shekhar Borkar, Intel Fellow and Director, Intel Corp., Hillsboro, OR

Robustness of Digital Circuits @ Low Voltage

Harry Veendrick, Research Fellow, Philips, Eindhoven, The Netherlands