

ISSCC TUTORIALS LIST

- ISSCC'02
- ISSCC'01
- ISSCC'00
- ISSCC'99
- ISSCC'98
- ISSCC'97
- ISSCC'96
- ISSCC'95

ISSCC'02 Tutorials

Tutorial 1: Specifications and Figures of Merit for Mixed-Signal Circuits – A Guide to Understanding Where the Numbers Come From and What They Mean

Instructor: David Robertson, Analog Devices, Inc.

Subcommittee: Analog

Tutorial 2: Design for Reliability in CMOS VLSI

Instructor: David Greenhill, Sun Microsystems UltraSparc, Sunnyvale, CA

Subcommittee: Digital

Tutorial 3: High-Dynamic-Range Image Sensors

Instructor: Abbas El Gamal, Stanford University, CA

Subcommittee: Imagers & MEMS

Tutorial 4: Ferroelectric Memory Design (FeRAM 101)

Instructor: Ali Sheikholeslami, Univ. of Toronto

Subcommittee: Memory

Tutorial 5: Architectures and Design Methods for Cryptography

Instructors: Ingrid Verbauwhede, Univ. of California-Los Angeles, CA

Instructors: Jim Goodman, Lumic Electronics, Ottawa, Canada

Subcommittee: Signal Processing

Tutorial 6: Introduction to Wireless-Receiver Design

Instructor: G. Tyson Tuttle, Silicon Labs, Austin, TX

Subcommittee: Wireless

Tutorial 7: CMOS Optical-Front-End Circuits

Instructor: Michel Steyaert, ESAT Lab, K.U. Leuven

Subcommittee: Wireline

ISSCC'01 Tutorials

Tutorial 1: Front-End Circuits for Optical Communications

Instructor: Yuriy M.Greshishchev, Nortel Networks, Ottawa, Canada

Subcommittee: Analog

Tutorial 2: Logical Effort – Designing Fast CMOS Circuits

Instructor: David Harris Harvey Mudd College, Claremont, CA

Subcommittee: Memory

Tutorial 3: Network Processing ICs

Instructor: C. Bernard Shung, Allayer Communications, San Jose, CA

Subcommittee: Signal Processing

Tutorial 4: Low-Power Design Techniques for Microprocessors

Instructor: Simon Segars, ARM Inc., Austin, TX

Subcommittee: Digital

Tutorial 5: Broadband Design for Wireless and Wired Systems

Instructor: Bud Taddiken, Microtune, Plano, TX

Subcommittee: Communications

Tutorial 6: Integrated Electronics for Displays

Instructors: Philip Alvelda, MicroDisplay, San Pablo, CA.

Instructors: Kai Schleupen, IBM, Yorktown Heights, NY

Subcommittee: Imagers & MEMS

For more detail see the Advance Program

(http://www.isscc.org/isscc/2001/ap/ap/AP_forWeb_Nov16.pdf)

ISSCC'2000 Tutorials

Tutorial 1: Analog CMOS Circuits for Baseband Receivers

Instructor: Paul Hurst, Professor, UC-Davis, CA

Subcommittee: Analog

Architecture options and design considerations for analog circuits in baseband receivers: AGC amplifiers, filters, adaptive and programmable equalizers, and sampling detectors. System requirements and options for A/D conversion.

Tutorial 2: Home Networking

Instructor: Gitty Nasserbakht, Proxim, Sunnyvale, CA

Subcommittee: Communications

Description of networked home and overview of promising networking technologies. An introductory overview of a various technologies including power-line, phone-line, and wireless solutions such as home RF and Bluetooth.

Tutorial 3: SOI Circuit Design Considerations

Instructor: Kerry Bernstein , IBM Microelectronics, Essex Junction, VT

Subcommittee: Digital

Partially-depleted silicon-on-insulator (PD-SOI) technology reduces CMOS circuit delay and power and creates design complexity. After review of SOI structure and device physics, responses and preferred design practices for static, dynamic and pass gate circuits are discussed, as well as specific circuits such as SRAMs, off-chip devices and PLLs, history effects, floating body effects, active parasitic elements, emerging SOI circuit topologies and impact of further scaling.

Tutorial 4: Design for Manufacturability of CMOS Image Sensors

Instructor: Albert Theuwissen , Philips Semiconductors, Eindhoven, The Netherlands

Subcommittee: Imagers & MEMS

There are differences between fabrication of analog or digital circuits in CMOS and fabrication of an imaging circuit. This tutorial reviews boundary conditions for design and layout of an imager taking into account functionality of the device and limits imposed by the available technology. Questions addressed include: How does technology influence performance? What is new in testing and packaging an imagers compared to standard CMOS devices? The tutorial includes costing and economics.

Tutorial 5: What is the Correct Package for my Integrated Circuit?

Instructor: DongHo Lee , Samsung, Yongin City, Korea

Subcommittee: Memory

Packaging technology has been developing rapidly during the last decade. The requirements of fast, small electronic devices drive packaging technology to deal with better thermal performance, smaller form factor, and higher noise immunity. The transition from lead-frame type packages to ball-array types is accelerated by high I/O counts and high-density surface-mount technology. To design or select an optimum package for the device, factors to be weighed include mechanical, electrical, and chemical considerations.

Tutorial 6: DSP Processors for Wireless Communications

Instructor: Chris Nicol , Bell Labs, Lucent Technologies, N. Ryde, Australia

Instructor: Ingrid Verbauwhede , Univ. of California, Los Angeles

Subcommittee: Signal Processing

Communication-specific requirements, such as filtering, voice coding and channel decoding are explained. Currently, two main evolutions can be distinguished: extremely-low-power DSP processors for handheld devices, and very-high-performance DSP processors for base stations. The design challenges of each class are illustrated with DSP processors from industry and academia.

ISSCC'99 Tutorials

Tutorial 1: Design Methodologies for Interconnect in GHz+ ICs

Instructor: Samuel Naffziger, HP Engineer/Scientist, Fort Collins, CO

Subcommittee: Digital

Specific impacts of interconnect RLC effects on digital IC design in the GigaHertz domain. Key analysis methods and tools, including R and 3D capacitance extraction and inductance analysis with emphasis on practical rules of thumb. Circuit solutions for mitigating the growing interconnect penalty, including repeaters, coupling noise management, wire/FET tradeoffs and signalling methods. Impact of the interconnect penalty on chip partitioning and micro-architecture.

Tutorial 2: Residential High-Bandwidth Access Technology

Instructor: Trudy Stetzler, Texas Instruments, Houston, TX

Subcommittee: Communications

Competing technologies are emerging to provide high-speed Internet access to the residential consumer. This tutorial provides a high-level overview of several of these technologies including cable, twisted pair (xDSL), wireless, and power-line modem access. A system-level explanation of each approach and a discussion of advantages and potential pitfalls of each technology are presented.

Tutorial 3: High-Speed CMOS ADCs

Instructor: Klaas Bult, Broadcom Corp., Irvine, CA

Subcommittee: Analog

50-400MHz 4-10b CMOS ADCs for embedded applications, dealing mainly with flash architectures with and without folding. Comparators and pre-amps are discussed. Averaging is used to improve accuracy without increased circuit complexity. After attaining a level of performance, interpolation and folding are used to reduce component count without loss of performance. A design example is given. Measured and published results are compared.

Tutorial 4: Video Compression Circuits

Instructor: Stephen Molloy, Luxxon Corp., San Jose, CA

Subcommittee: Signal Processing

An introduction to circuits for MPEG encoding/decoding: discrete cosine transform, motion compensation, quantization, entropy coding, bitstream packing/unpacking. Circuits for alternative coding schemes: wavelet/subband filterbanks. High speed and low power implementations.

Tutorial 5: Single-Chip CMOS Imaging System

Instructor: Hon-Sum Philip Wong, IBM T. J. Watson Research Center, Yorktown Heights

Instructor: Abbas El Gamal, Assoc. Prof., Stanford University, CA

Subcommittee: Imagers & MEMS

Overview of single-chip CMOS imaging systems, from fabrication technology to pixel and system architecture. The tutorial follows the signal path of a single-chip CMOS imaging system, photon conversion to voltage, pixel architectures, sensor performance measures, A/D conversion, color processing, and on-chip image processing, and impact of CMOS device and technology scaling on CMOS image sensor performance. R&D trends are summarized.

Tutorial 6: Signaling in High-Performance Memory Systems

Instructor: John Poulton, Research Prof., Dept. of Computer Science, Univ. of North Carolina at Chapel Hill

Subcommittee: Memory

Transmission line characteristics, termination methods, noise sources and coupling, signal levels, current-mode, voltage-mode, single-ended and differential signaling, clocking, references. Characteristics of busses, packaging considerations, limitations on

bus signaling speed. Bus-based memory signaling, including RDRAM, SLDRAM, DDR, PC100. Improving memory signaling.

ISSCC'98 Tutorials

Tutorial 1: High-Speed SRAM Design

Instructor: Bruce Bateman, MicroUnity Systems Engineering, Sunnyvale, CA

Subcommittee: Memory

Memory cell types, design and scalability. High-speed memory architecture. Fanout-dominated design techniques and decoding structures. High-speed sensing and related noise considerations. Writing circuits. Redundancy. Async vs Sync designs. Embedded arrays. Multi-port and pseudo-multi-port designs. Reliability.

Tutorial 2: How a Spread-Spectrum Radio Works

Instructor: Charles Chien, Rockwell Science Center

Subcommittee: Communications

Spread-Spectrum in wireless systems, including next-generation digital cellular, personal communications, and wireless local area networking. Comprehensive treatment of architecture and circuits design of complete spread-spectrum radios with RF front-end, digital modem, and network interface. Topics include wireless channel models, spread-spectrum communications, digital modem circuits, RF front-end architectures, and example systems such as IS-95.

Tutorial 3: Opamp Compensation for Low-Voltage, Mixed-Signal Designs

Instructor: John W. Fattaruso, Texas Instruments, Dallas, TX

Subcommittee: Analog

As power-supply voltages are reduced, trends in opamp design for mixed-signal systems are toward multiple non-cascode stages. Frequency-compensation techniques applicable to three- and four-stage amplifiers are covered. After a review of basic pole-splitting, nested Miller and nested Gm-C compensation are described. Practical CMOS designs are presented.

Tutorial 4: FIR-1001: Architectures and Applications

Instructor: Mehdi Hatamian, Broadcom Corp., Irvine CA

Subcommittee: Signal Processing

FIR filter architectures, implementation trade-offs, high-speed filters, layout issues, pipelining techniques, programmable fixed-coefficient and adaptive FIRs, decision-

feedback equalizers, applications in communication, examples.

Tutorial 5: MEMS for the Circuit Designer

Instructor: Khalil Najafi, Associate Professor of EECS at University of Michigan.

Instructor: William Kaiser, Chairman of the UCLA EE Dept

Subcommittee: Sensors & Imagers

This two-part tutorial provides circuit designers with background for developing systems combining circuits and MEMS. It first reviews current and future applications, including micromachined sensors, MEMS tunable RF communication devices, microoptical systems on a chip, microfluidics, and biomedical systems. It then focuses on fundamental limits of CMOS interface circuits, and their challenges and implementation. The tutorial concludes with analysis of the microgyroscope interface system and future opportunities.

Tutorial 6: High Speed Clocking for Large Digital ICs

Instructor: John Maneatis, at Silicon Graphics, Mountain View, CA

Subcommittee: Digital

Clocking for large high-speed synchronous digital designs, including clock generation, phase-locked loops, clock distribution, clock gating, skew management, skew budgeting, latch and register design, setup and hold-time, testability issues, and logic pipeline approaches, from simple register to multiphase-latch-based designs, using static and precharged logic. Clocking overhead minimization techniques necessary at clock frequencies approaching 1GHz.

ISSCC'97 Tutorials

Tutorial 1: Practical Design for Analog Discrete-Time Processing (ADTP)

Instructor: Donald Kerth, Crystal Semiconductor, Austin, TX

Subcommittee: Analog

Introduction to the operating principles of basic circuits for discrete time analog processing. Design and analysis techniques for the practical applications to CMOS switched-capacitor circuits, including SD modulators, algorithmic ADCs, and switched-capacitor filters. Issues of psrr, noise, charge injection, amplifier topology, and digital noise interference.

Tutorial 2: Clock and Data Recovery for Serial Digital Communications (CR)

Instructor: Richard Walker, Hewlett-Packard Labs

Subcommittee: Communications

Techniques for data transmission over serial optical and electrical links. The common distortions that occur over such links. Eye diagrams, jitter tolerance, jitter transfer

function, and jitter generation. Data encoding for run length control, framing, and dc-balance. Clock recovery for monolithic implementation including PLL components such as data-driven phase/frequency detectors and charge pumps.

Tutorial 3: Microprocessor Architecture: RISC Evolution into Super-Scalars (uP)

Instructor: Vojin Oklobdzija, UC Davis, CA and Integration, Berkeley, CA

Subcommittee: Digital

Guiding principles of modern microprocessor architecture. Basis of RISC architecture and relation to micro-architecture and pipelining for high-performance implementation. The next step, super-scalar implementations, is explained with respect to performance and difficulties of implementation. The super-scalar pipeline is contrasted to vector and VLIW machines.

Tutorial 4: New DRAM Architectures (DRAM)

Instructor: Steven Przybylski, Consultant

Subcommittee: Memory

Semiconductor and computer system trends explain the current explosion in number of DRAM architectures and fundamental challenges facing system and DRAM designers at 256Mb and 1Gb densities. Technical and business strengths and weaknesses of: EDO DRAMs, SDRAMs, RDRAMs, SLDRAMs, and MDRAMs.

Tutorial 5: Making MEMS Real: Beyond the Microstructure (MEMS)

Instructor: Jean-Paul Bardyn, CSEM, Neuchatel, Switzerland

Subcommittee: Sensors and Imagers

Brief overview of micromachining technologies and sensing mechanisms. Circuit architectures and associated performance limitations of IC/sensor interface. Interfacing of micromachined capacitive accelerometers, including S/N ratio vs. power dissipation analysis. Challenges facing the IC designer of MEMS.

Tutorial 6: Circuit and Technology Trends for Low-Power/High-Performance DSP (DSP)

Instructor: Anathan Chandrakasan, MIT, Cambridge, MA

Subcommittee: Signal Processing

Reduced-swing bus drivers. Embedded (variable) power supply systems: system architecture, asynchronous vs. synchronous, high-efficiency variable voltage dc-dc conversion and voltage quantization, averaging, and algorithm design. Low-voltage (<1V) high-speed: multiple-threshold CMOS, substrate biasing, dual-gate SOI and dynamic threshold CMOS.

ISSCC Tutorials'96

Tutorial 1: Monolithic Phase-Locked Loops

Instructor: Behzad Razavi, AT&T Bell Labs, Holmdel, NJ

Subcommittee: Analog

Why phase-lock? Basic concepts, operating principles and limitations of a simple PLL; loop dynamics; design of building blocks (VCOs, phase/frequency detectors, charge pumps) in CMOS and bipolar technologies; noise in PLLs; applications in wireless and digital systems.

Tutorial 2: Techniques for Low-Power Digital Signal Processing

Instructor: Anantha P. Chandrakasan, MIT, Cambridge, MA

Subcommittee: Signal Processing

Circuits and architectures. Voltage reduction techniques: concurrency-based architecture scaling and device optimization. Efficient dc-dc conversion for low-voltage operation. Reduced-swing logic and adiabatic charging lower energy at a fixed supply. Minimizing switched capacitance: operation reduction, optimizing data representation and signal correlations, minimizing spurious transitions, optimizing sequencing of operations, activity-driven power down, and optimizing arithmetic structures and circuits.

Tutorial 3: Micromachined Sensors

Instructors: Dennis L. Polla, Univ. of Minnesota, Minneapolis, MN

Gregory T. A. Kovacs, Stanford University, Stanford, CA

Subcommittee: Sensors & Imagers

Advances in micromachining, thin-film materials, and IC process integration open opportunities in a variety of fields. Common transduction mechanisms realized on a semiconductor chip: mechanical, optical, magnetic, thermal, chemical, and biological sensing. Overview of micromachining technologies. Discussion of sensing, actuation and systems integration.

Tutorial 4: Dynamic Logic: Clocked and Asynchronous

Instructor: Ted Williams, Silicon Graphics, Mountain View, CA

Subcommittee: Digital

Characteristics and performance of precharge, postcharge, self-resetting, single-edge, and domino chain dynamic logic. Where to use and interface these techniques. Choices for clocked and dual-rail self-clocked latches, how latches follow or combine with dynamic logic, and how to control when dynamic portions reset in clocked and self-timed

pipelines. Charge-sharing, noise margin, power use, latency, throughput, and area trade-offs.

Tutorial 5: RF ICs for Cellular and Cordless Telephones

Instructor: Paul Davis, AT&T Bell Labs, Reading, PA

Subcommittee: Communications

0.8-2.0GHz RF IC subcircuits (amplifiers, mixers, phase shifters, and oscillators) in context of selected cellular and cordless radio system requirements. Transmitter, receiver, and synthesizer architectures and subcircuits addresses requirements such as RF sensitivity, interference rejection, and spurious signals. Emphasis is on RF bipolar analog ICs.

Tutorial 6: Nonvolatile Memory Design

Instructor: Jagdish Pathak, Sub Micron Circuits, Los Altos Hills, CA

Subcommittee: Memory

Memory cells, layout, and architecture. Evolution of nonvolatile memories from ROM to Flash. Cell operation and disturbs for different architectures. High- and low-voltage circuits and isolation, high-speed design in arrays, and designing around these limitations. High-voltage generation and charge-pump design. Definition and purpose of test modes for in-house testing.

ISSCC95 Tutorials

Tutorial 1: Introduction to Oversampled Data Conversion

Instructor: Richard Hester, TI Fellow, Texas Instruments, Dallas, TX

Subcommittee: Analog

Introduction to oversampled data conversion. Explanation of quantization noise and development of noise-shaping concept. Various oversampled converter technologies compared in terms of quantization, limit-cycle-oscillation energy, and stability. On-going research is identified.

Tutorial 2: Clocking for High-Performance Processors

Instructor: Mark Horowitz, Assoc. Prof., Stanford University, Stanford, CA

Subcommittee: Digital

Role of the clock in a digital system, how clocks sequence events in the processor, how processor architecture/implementation makes clock design difficult, various approaches to solving problems from removing clocks entirely (asynchronous design), to brute-force methods of making clocking work, to using PLLs. None of these approaches is perfect, but many can be made to work for processors running at hundreds of MHz.

Tutorial 3: Introduction to RF Communication Systems and Circuits

Instructor: William J. Ooms, Research Manager, Integrated Electronics Research, Motorola Inc., Tempe, AZ

Subcommittee: Communications

Broad overview of basic elements of radio-communication circuits and associated RF circuits. The target audience is digital engineers, managers, and others with little or no familiarity with radio circuits and systems. Emphasis is on defining relevant "RF jargon" and terms in common use among RF designers.

Tutorial 4: Cache Memory

Instructor: Roy Flaker, Senior Technical Staff Member, IBM, Burlington, VT

Subcommittee: Memory

Basic understanding of cache memory concepts: overview and history of cache memory, basic architectural concepts for first- and second-level caches, examples of cache circuits illustrate the state of the art. Focus is on CMOS embedded-cache circuits. Future cache-design directions considering processor demands for higher performance and lower power.

Tutorial 5: Image Sensors: On-Ramps to the Digital Highway

Instructors: David F. Barbe, Professor of EE, Univ. of Maryland, College Park, MD
Charles V. Stancampiano, Device Engr., Eastman Kodak Co., Rochester, NY

Subcommittee: Sensors & Imagers

Fundamental concepts in modern solid-state imaging chips: historical overview of solid-state imaging, basic functions that imagers perform (sensing, integration, transfer, readout), sensor types (CCD, MOS, photodiode), array organizations (line and area, including frame, interline and FIT), performance characteristics (resolution, response, output rates, color, blooming, smear, lag). Examples of state-of-the-art imagers for camcorder, HDTV and custom applications.

Tutorial 6: Hard-Disk-Drive Signal Processing (4:30 - 6:00)

Instructor: Richard G. Yamasaki, Corporate Fellow, Silicon Systems, Tustin, CA

Subcommittee: Signal Processing

Signal processing in magnetic hard-disk drives: equalization, data coding, write precompensation, and partial-response signaling for combating intersymbol interference. PRML, EPR4, and EEPR4 channels with dynamic-threshold, Viterbi and sample-look-ahead maximum-likelihood detectors. Advanced channels vs. present peak-detection. Analog vs. digital processing and future trends.

